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| 10/620,859 | 07/15/2003 | Lakhbeer S. Sidhu | A1064 | 9135 |

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| ART UNIT | PAPER NUMBER |
|---|---|
| 2832 | |

DATE MAILED: 01/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/620,859 | SIDHU ET AL. | |
| | Examiner | Art Unit | |
| | Anh T. Mai | 2832 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16,22-26 and 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,22-26 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. Claim 7 is objected to because of the following informalities: limitation "the length of the via-trench *conductive line* is equal to the length of the via-trench *conductive lines*" appears to be incorrect. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-5, 7, 27, are rejected under 35 U.S.C. 102(b) as being anticipated by Ewen et al. [5446311].

Ewen discloses three metal conductor lines M1, M2, M3 running parallel to each other in respective metal layer dielectric layers 2,4,8 in interconnect dielectric stack; at least one via-trench via line 9 in a via trench dielectric layer wherein the via-trench conductive line lies between two metal layers.

With respect to claim 3, the metal conductive lines, each forms a spiral between first and second terminals [figures 1-3; col 2, lines 10-35].

With respect to claims 4-5, Ewen discloses three vertical conductive line and there are two sets of via trench 9 between M1/M2 and M2/M3 as shown in figure 3.

With respect to claim 7, each via 9 has a length that is equal to the length of via conductive lines.

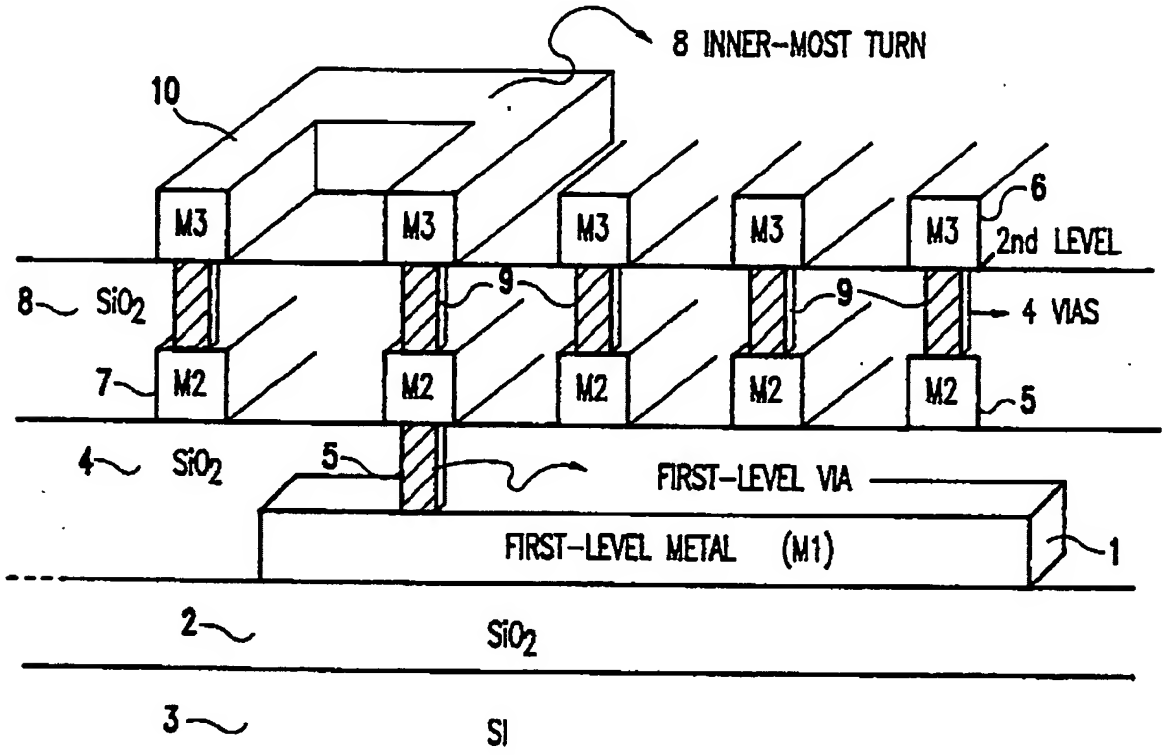


FIG.3

*Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 22-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Niitsu [2002/0158306].

Nittsu discloses method of forming integrated inductor circuit with dielectric interconnect stack 15,35,55; forming at least two vertically-aligned conductive lines 40,20 in the dielectric using damascene process, via 30 run between conductive lines 20,40 [figure 2B, paragraph 0039]

**[0039]** Note that the spiral inductor **20** and the electromagnetic wave shield **60** according to the first embodiment can be formed by use of a manufacturing method generally used for manufacturing a semiconductor device. For example, the spiral inductor **20** and the electromagnetic wave shield **60** may be formed by use of, for example, a damascene process or a dual damascene process as described below. Hereinafter, description will be made for an example of a fabrication method thereof with reference to **FIG. 2B**.

4. Claim 30 is rejected under 35 U.S.C. 102(e) as being anticipated by Hsu [2003/0234436A1].

Hsu discloses interlayer dielectric stack 58,64,70,76,80,86 lies on a surface of semiconductor substrate 46 comprising two metal layer conductive lines 62,68, that run parallel to each other in respective to dielectric layer of the stack, a conductor via trench 66 electrically connects the two metal layer conductive lines; a region of shallow trench isolation 50 forming on the surface of the substrate and under metal layers [figure 2].

[0029] **FIG. 2** is a sectional view of one embodiment of the present invention which includes a semiconductor device **10** having an inductor **11**. The semiconductor device **10** includes a body portion **12** which may include a silicon based substrate **46** into which a N or P-well is formed as well as a shallow trench isolation region **50**. A discrete device **52** may be formed in portions of the silicon based substrate **46**. An interlayer dielectric **58** may be formed over the discrete devices **52** and electrically conductive plugs **60** may be formed through the interlayer dielectric **58** connecting to active regions **54, 56** of the discrete device **52**. A first layer metallization **62** may be formed over the interlayer dielectric **58**. A first inter-metal dielectric **64** may be formed over the first metallization layer **62** and electrically conductive plugs **66** may be formed through the first inter-metal dielectric layer **64** down to the first metallization layer **62**. A second inter-metal dielectric **68** may be formed over the first inter-metal dielectric **64**. A second inter-metal dielectric **70** may be formed over the second metallization **68** and a plug **72** formed through the second inter-metal dielectric **70** down to a second metallization layer **68**. A third metallization layer **74** may be formed over the second inter-metal dielectric layer **70**. A third inter-metal dielectric **76** may be formed over the third metallization **76** and a plug **78** formed through the third inter-metal dielectric **76** down to the third metallization **74**. A fourth metallization **18** may be formed over the third inter-metal dielectric layer **76**. A fourth inter-metal

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 8-10, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ewen in view of Sia et al.

Ewen discloses the invention as claimed as cited above except for the conductor lines being made of copper. Sia discloses copper as conductive material for his invention. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use copper as conductive material as taught Sia to conductive material as disclosed by Ewen. The motivation would have been to use alternative materials that are available to perform the electrical requirement for the device.

With respect to claims 8-9, 29 limitation "damascene and dual-damascene semiconductor fabrication process" has been considered but not given any patentable weight because it's a product by process claim. During the examination, the patentability of a product-by-process claim is determined by the novelty and nonobviousness of the claimed product itself without consideration of the process for making it, which is recited in the claim. *In re Thorpe, 227 USPQ 964 (Fed cir. 1985).*

With respect to claim 10, Sia discloses a stack inductor having top dielectric layer 150' and top conductive line 24/26 is formed in the top dielectric layer [see figure 2].

6. Claims 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ewen in view of Tisharo et al. [5515022].

Ewen discloses the claimed invention as cited above except for the via-trench having bottom width less than upper width. Tisharo discloses via 35 having cross shape shows the width of the upper is larger than that of the lower [figure 2; col 6, lines 30-39]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have tapering

shape of the via as taught by Tisharo to Ewen. The motivation would have been to improve large-scale production and product yield and to reduce performance variation and change with time [col 6, lines 37-39]. Therefore, it would have been obvious to combine Tisharo with Ewen.

7. Claim 11 is rejected under 35 U.S.C. 103(a) in view of Ewen.

Ewen discloses the claimed invention except for the concave upper surfaces of the conductive lines. It is obvious that the concave upper surface and convex lower surface are caused by dishing effect during the fabrication process whereas the softness of copper metal lines as disclosed by applicant in the specs, page 4, lines 20-30.

8. Claim 12 is rejected under 35 U.S.C. 103(a) in view of Ewen in view of Niitsu [2002/0128306A1].

Ewen discloses the claimed invention as cited above except for a metal plate between the two metal layers conductive line and the substrate.

Nittsu discloses metal shield 12 disposed between the two metal layer conductive lines 20,30 and surface of substrate 10 [figure 3B; paragraphs 0046-0047]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use a metal plate positioned between metal layers conductive lines and the surface of semiconductor substrate as taught by Niitsu to the inductor as disclosed by Ewen for the purpose of maintain the self-inductance of the inductor and deterioration of Q value can be prevented [page 4, paragraph 51, last sentence]. Therefore, it would have been obvious to combine Niitsu with Ewen.

9. Claims 13-14, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ewen in view of Gillespie [6798039].

Ewen discloses the claimed invention as cited above except for n-type/p-type wells at the surface of substrate that forms a plurality of reversed bias diodes that block eddy currents.

Gillespie discloses the alternating regions of implanted n-well and p-well impurities in the substrate underneath the inductor or by reversing p-n junctions underneath the inductor to minimizing eddy currents [col 3, lns 11-16]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use n-well, p-well at the surface of semiconductor substrate as taught by Gillespie to the inductor as disclosed by Ewen to reduce Eddy Current flowing in the substrate. Therefore, it would have been obvious to combine Gillespie with Ewen.

> In FIG. 4A, a plan view of alternating N-type and P-type well regions 40 is provided. These alternating well regions provide a high resistance path in a semiconductor substrate (e.g., bulk semiconductor substrate). This high resistance path operates to reduce eddy currents within a semiconductor substrate when used in conjunction with an inductor according to an embodiment of the present invention. An exemplary inductor may include a plurality of primary strand segments 42 that are concentrically arranged. These N-type and P-type well regions are preferably elongate regions that extend in a lengthwise direction. This lengthwise direction is at least substantially orthogonal (e.g., ≧45°) to the plurality of primary strand segments. In FIG. 4B, which represents an enlarged plan view of a portion of the alternating regions illustrated by FIG. 4A, the P-type well regions are illustrated as being electrically coupled together at multiple locations. These P-type well regions may be formed within a deeper N-type well region. Eddy current losses can also be reduced by defining an inductor using uppermost levels of metallization that are relatively distant from the substrate.

With respect to claim 16, Ewen in view of Gillespie does not disclose the size of the lateral spiral of less than 200 microns. It would have been obvious to select the dimension of the inductor as the matter of choice to satisfy the desired performance of the device. *In Gardner v. TEC Systems, Inc. , 725 F.2d 1338, 220 USPQ 777* (Fed.Cir. 1984),

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ewen in view of Gillespie as applied in claim 13 above and further in view of Hsu.

Ewen in view of Gillespie discloses the claimed invention except for an region of shallow trench isolation [STI] formed on the surface of the substrate. Hsu discloses interlayer dielectric stack 58,64,70,76,80,86 lies on a surface of semiconductor substrate 46 comprising two metal layer conductive lines 62,68, that run parallel to each other in respective to dielectric layer of the stack, a conductor via trench 66 electrically connects the two metal layer conductive lines; a region of shallow trench isolation 50 forming on the surface of the substrate and under metal layers [figure 2].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have region of isolation at the surface of semiconductor substrate as taught by Hsu to the inductor as disclosed by Ewen in view of Hsu. The motivation would have been to increase spacing between the conductors and the substrate.

11. Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Gillespie.

Hsu discloses the claimed invention as cited above except for n-type/p-type wells at the surface of substrate that forms a plurality of reversed bias diodes that block eddy currents. Gillespie discloses the alternating regions of implanted n-well and p-well impurities in the substrate underneath the inductor or by reversing p-n junctions underneath the inductor to minimizing eddy currents [col 3, lns 11-16]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use n-wells, p-wells as taught by Gillespie to

the surface of semiconductor substrate as disclosed by Hsu to reduce Eddy Current flowing in the substrate. Therefore, it would have been obvious to combine Gillespie with Hsu.

With respect to claim 33, Hsu show a spiral inductor in figure 1.

*Response to Arguments*

12. Applicant's arguments with respect to claims 1-16, 22-27, 29-33 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh T. Mai whose telephone number is 571-272-1995. The examiner can normally be reached on 5/4/9 Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on 571-272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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